REMARKS

Applicant notes that the Office Action only refers to claims 1-6. As no claims have been cancelled, and originally claims 1-7 were presented, Applicant assumes the reference of only claims 1-6 is an oversight and responds as if the Office Action made a typographical error. Claims 1-7 were examined and reported in the Office Action. Claims 1-7 are rejected. Claim 1 is amended. Claims 1-7 remain

Applicant requests reconsideration of the application in view of the following remarks.

I. 35 U.S.C. §112, Second Paragraph

It is asserted in the Office Action that claim 1 is rejected under 35 U.S.C. §112, second paragraph, due to lack of antecedent basis and ambiguities. Applicant has amended claim 1 to overcome the 35 U.S.C. §112, second paragraph, rejection.

Accordingly, withdrawal of the 35 U.S.C. §112, second paragraph, rejections for Claim 1 are respectfully requested.

II. 35 U.S.C. §102(b)

It is asserted in the Office Action that claims 1-7 are rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,525,549 issued to Fukada et al. ("Fukada"), U.S. Patent No. 4,975,390 issued to Fujii et al. ("Fujii"), U.S. Patent No. 6,130,010 issued to Ishio et al. ("Ishio"), or U.S. Patent No. 6,250,165 issued to Sakai et al. ("Sakai"). Applicant respectfully disagrees.

According to MPEP 2131, "'[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.' (Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987)). 'The identical invention must be shown in as complete detail as is contained in the ... claim.' (Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989)). The elements must be arranged as required by the claim, but this is not an ipsissimis verbis test, i.e., identity of

terminology is not required. (In re Bond, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990))."

Applicant's amended claim 1 contains the limitations of "[a] semiconductor pressure sensor comprising: a silicon substrate (1) with a main surface side and a diaphragm (10) which produces a distortion depending on a pressure; strain gauges (5a, 5b, 5c, 5d) which are provided on the main surface side of the silicon substrate (1) with the diaphragm (10) and are formed by conductive diffusion resistors different from said substrate; and a getter (8) which is provided on the main surface side of the silicon substrate (1) including a periphery of the getter adjacent to said strain gauges (5a, 5b, 5c, 5d), said getter comprising the PN-junction area to which reverse bias is impressed so that metal impurities may be captured which are contained in the silicon substrate, and which contain at least an Fe atom."

Applicant's claimed invention prevents the adhesion of the metal ion to the sensor pattern, which otherwise becomes a problem in a silicon pressure sensor. Since there is a strong likelihood that iron (Fe) ion is greatly involved in the fluctuation of a processing signal, Applicant's claimed invention absorbs the Fe ion with a getter. The getter is provided in the vicinity of the sensor pattern. According to Applicant's claimed invention, the manufacturing method of the sensor with a getter has been realized by impressing the reverse bias to the same P type pattern as a sensor pattern.

Applicant notes that the problem solved by Applicant's claimed invention is a not addressed by any of the cited prior art references. That is, none of the cited prior art references ever discovered the problem and, therefore, could not possibly have taught, suggested or disclosed Applicant's claimed invention, which solves the above-mentioned problem. Moreover, since the discovery of the problem is new, it follows that the solving of the problem must also be new.

Fukuda discloses a method for producing a semiconductor device that can solve problems related to dicing a metal thin film used for electrochemical etching. Although Fukada discloses that the reverse bias is used with an etching stopper, the reverse bias area is not provided in the vicinity of the sensor 107. The structure of Fukada's disclosed invention and the problem solved are thus distinguishable from Applicant's

claimed invention. Fukada does not disclose, teach or suggest knowing of the problem related to Fe ion's effect on processing signal fluctuation, nor does Fukada disclose, teach or suggest solving the same.

Sakai discloses semiconductor physical quantity sensor. According to Sakai, it is necessary to make a cavity inside a substrate in making the structure of an acceleration sensor. Distinguishable, according to Applicant's claimed invention, etching is controlled by the reverse bias. Sakai does not disclose, teach or suggest knowing of the problem related to Fe ion's effect on processing signal fluctuation, nor does Sakai disclose, teach or suggest solving the same.

Fujii discloses a semiconductor pressure sensor. Fujii does not disclose, teach, or suggest reverse bias. Moreover, Fujii does not disclose, teach or suggest knowing of the problem related to Fe ion's effect on processing signal fluctuation, nor does Fujii disclose, teach or suggest solving the same.

Ishio discloses a semiconductor dynamic sensor having the PN-junction that uses an anisotropic etching mask. Ishio does not disclose, teach, or suggest reverse bias. Moreover, Ishio does not disclose, teach or suggest knowing of the problem related to Fe ion's effect on processing signal fluctuation, nor does Ishio disclose, teach or suggest solving the same.

Therefore, since neither Fukada, Fujii, Ishio, nor Sakai disclose, teach or suggest all of Applicant's amended claim 1 limitations, Applicant respectfully asserts that a *prima facie* rejection under 35 U.S.C. § 102(b) has not been adequately set forth relative to either Fukada, Fujii, Ishio, or Sakai. Thus, Applicant's amended claim 1 is not anticipated by either Fukada, Fujii, Ishio, or Sakai. Additionally, the claims that depend directly or indirectly on claim 1, namely claims 2 -6, are also not anticipated by either Fukada, Fujii, Ishio, or Sakai for the above same reason.

Accordingly, withdrawal of the 35 U.S.C. § 102(b), rejections for claims 1-7 are respectfully requested.

III. Claims Rejected Under 35 U.S.C. §103

It is asserted in the Office Action that claims 1-7 are rejected under 35 U.S.C. §103(a) as being unpatentable over Fukada, Fujii, Ishio, or Sakai, each in view of no other prior art. Applicant respectfully disagrees.

According to MPEP §2142 "[t]o establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." (In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)). Further, according to MPEP §2143.03, "[t]o establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. (In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974)." "All words in a claim must be considered in judging the patentability of that claim against the prior art." (In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970), emphasis added).

Applicant discusses amended claim 1 with respect to Fukada, Fujii, Ishio, and Sakai above in section II.

As discussed above, neither Fukada, Fujii, Ishio, nor Sakai disclose all of Applicant's amended claim 1 limitations. Moreover, neither Fukada, Fujii, Ishio, or Sakai disclose, teach or suggest knowing of the problem related to Fe ion's effect on processing signal fluctuation, nor does either Fukada, Fujii, Ishio, or Sakai disclose, teach or suggest solving the same.

Therefore, since neither Fukada, Fujii, Ishio, nor Sakai disclose, teach or suggest all the limitations contained in Applicant's amended claim 1, as listed above, there would not be any motivation to arrive at Applicant's claimed invention. Thus,

Applicant's amended claim 1 is not obvious over Fukada, Fujii, Ishio, or Sakai, each in view of no other prior art since a *prima facie* case of obviousness has not been met under MPEP §2142. Additionally, the claims that depend directly or indirectly from Applicant's amended claim 1, namely claims 2-7, are also not obvious over Fukada, Fujii, Ishio, or Sakai, each in view of no other prior art for the above same reasons.

Accordingly, withdrawal of the 35 U.S.C. §103(a) rejection for claims 1-7, are respectfully requested

CONCLUSION

In view of the foregoing, it is submitted that claims 1-7 patentably define the subject invention over the cited references of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes a telephone conference would be useful in moving the case forward, he is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR, & ZAFMAN LLP

Dated: 11/7/03

By _____
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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail with sufficient postage in an envelope addressed to: Mail Stop Non-Fee Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450 on November 7, 2003.

Nadya Gordon 11/7/03
Nadya Gordon Date

MARKED-UP VERSION

~~Semiconductor pressure sensor~~SEMICONDUCTOR PRESSURE SENSOR WITH STRAIN GAUGES FORMED ON A SILICON DIAPHRAGM

BACKGROUND

~~1. Technical Field~~Field

[0001] This invention relates to a semiconductor pressure sensor. More specifically, the present invention is directed to a semiconductor pressure sensor of the type ~~which~~ that uses strain gauges formed on a silicon diaphragm.

~~2. Background Art~~ Background

[0002] Conventionally, a semiconductor pressure sensor using strain gauges is known. The pressure sensor forms a pressure-sense diaphragm on a silicon substrate. And, sensor elements (piezo-resistive devices) comprised by diffusion resistor ~~layer~~ layers are provided on the pressure-sense diaphragm. The variation of a pressure is measured by the detection of the distortion in the diaphragm.

[0003] **Fig. 7** is a perspective diagram showing a semiconductor pressure sensor using conventional strain gauges. A part of the pressure sensor is shown by the cross section view. As shown in **Fig. 7**, ~~a~~ sensor chip 200 is made by ~~a~~ silicon base 101, which has ~~a~~ diaphragm 110, and sensor elements on ~~the~~ diaphragm 110. ~~The diaphragm~~Diaphragm 110 provides the whole center section of ~~the~~ silicon base 101 with a thin film, excluding a circumference part. ~~A~~ Wheatstone Bridge circuit 113 is comprised by strain gauges 105a-105d made from diffusion resistors, ~~a~~ metal wiring 103, and terminals 104a-104d.

[0004] **Fig. 8** is a circuit diagram showing ~~the~~ Wheatstone Bridge circuit 113 based on **Fig. 7**. As shown in the diagram, ~~the~~ strain gauges 105a-105d made from diffusion resistors are respectively connected by ~~the~~ metal wiring 103. Terminals 104a-104d are provided between each strain gauge. Terminal 104a is connected to a power supply (high potential side). Moreover, terminal 104c is connected to a ground (low potential side). Therefore, a variation of resistance in strain gauges 105a-105d is

performed by the deformation of ~~the~~ diaphragm 110 of **Fig. 7**. The voltage value between terminals 104b and 104d varies. The variation of a pressure is measured by the detection of change in voltage.

[0005] In the meantime, ~~the~~ sensor chip 200 is fixed on ~~a~~ pedestal 111, such as Pyrex™ ~~(TM)~~ glass. And, ~~the~~ sensor chip 200 is sealed in a package together with a silicon sealing liquid. ~~The pedestal~~Pedestal 111 provides ~~a~~ through-hole 112 for extracting air. ~~The sensor~~Sensor chip 200 is attached so that ~~the~~ through-hole 112 may be covered. The silicon sealing liquid (not illustrated) is maintained on ~~the~~ diaphragm 110. The sensor elements on ~~the~~ diaphragm 110 (each member which comprises ~~the~~ Wheatstone Bridge circuit 113) is isolated from an external field. Therefore, the variation of a pressure is transmitted to the sensor elements via the silicon sealing liquid.

~~3. Disclosure of Invention~~[Problem to be solved]

[0006] The pressure sensor (as shown above) needs a fine pattern process ~~of~~n the silicon substrate for formation of the diaphragm and the diffusion resistors, and is made from the semiconductor manufacturing process, which must be considered sufficiently dustproof. However, even though the present clean room provides means for preventing dust, a trace metal-impurity enters into a wafer or is generated midway through a process. As a result, the metal-impurity may bring on a fluctuation in a sensor output.

[0007] In general, when various semiconductor devices, such as MOSFET or the like, are manufactured, a removal in the influence of a device, etc. is performed by capturing the metal-impurity during the manufacturing process of the wafer. This is called gettering. From the difference ~~of~~ in the principle, it is classified into a EG (extrinsic gettering) method and a IG (intrinsic gettering) method. The EG method is the technique ~~which~~that roughens a wafer back-side using a sandblasting method, etc. to collect the impurity in the roughened-surface. The IG method is the technique ~~which~~that makes many micro defects inside the wafer ~~many micro defects~~ by precipitates of oxygen to capture the impurity in the micro defects.

[0008] However, the semiconductor pressure sensor with the structure ~~which~~ that provides the strain gauges on the diaphragm etches most silicon-substrate back-sides to form the diaphragm. For this reason, even though gettering is performed in the wafer using the conventional EG ~~method~~ and IG methods, a getter reduces at the time of a formation of the diaphragm. Therefore, it becomes difficult to capture the impurity sufficiently. Moreover, a new process for making the getter is required. There is also a problem that an effect changes with varieties of the wafer (a bare substrate, SOI (Silicon On Insulator) substrate, epitaxial substrate, etc.).

[Means for solving the problem]

[0009] The invention is made in order to solve ~~such~~ the above-mentioned~~a~~ problem, and an object of the present invention is to provide a semiconductor pressure sensor in which fluctuation in a sensor output is difficult to be produced.

[0010] A semiconductor pressure sensor, according to the present invention, comprises ~~a~~ Silicon substrate (1) with ~~a~~ diaphragm (10) ~~which~~ that produces a distortion depending on a pressure, strain gauges (5a, 5b, 5c, 5d) ~~which~~ that are provided on ~~the~~ diaphragm (10) and are formed by diffusion resistors, and a PN-junction area ~~which~~ that is provided adjacent in ~~the~~ strain gauges (5a, 5b, 5c, 5d) and ~~which~~ that the reverse bias is applied to.

[0011] The PN-junction area may comprise the boundary surface between ~~the~~ silicon base (1) and ~~a~~ diffusion layer (8) provided in ~~the~~ silicon base (1).

[0012] ~~The diffusion~~Diffusion layer (8) may be locally provided near ~~the~~ strain gauges (5a, 5b, 5c, 5d).

[0013] A plural pair of strain gauges (5a, 5b, 5c, 5d) may be provided.

[0014] ~~The plural~~Plural strain gauges (5a, 5b, 5c, 5d) may form Wheatstone Bridge circuits.

[0015] The PN-junction area may be provided only in ~~the~~ strain gauge (5c) at the side of the large electrical potential difference with a substrate potential among ~~the~~

terminal (4a) at the side of a high electric potential in the Wheatstone Bridge circuit and the terminal at the side of ~~a~~ low potential (4c).

[0016] ~~The diffusion~~Diffusion layer (8) may be formed of the combination of the plural long and slender patterns ~~which~~ that are ~~an~~ acutely angled toward ~~the~~ strain gauges (5a, 5b, 5c, 5d).

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] ~~4. Brief Description of Drawings~~ **Fig. 1** is a top view ~~-~~showing a semiconductor pressure sensor according to Embodiment 1 of the present invention.

[0018] **Fig. 2A** is a sectional view taken in ~~the~~ line A-A' in ~~FIG~~**Fig. 1**. **Fig. 2B** is a sectional view taken in ~~the~~ line B-B' in **Fig. 1**.

[0019] **Fig. 3** is a top view showing Embodiment 2 of the present invention.

[0020] **Fig. 4** is a top view showing Embodiment 3 of the present invention.

[0021] **Fig. 5** is a top view showing Embodiment 4 of the present invention.

[0022] **Figs. 6A, 6B,** and **6C** are the top views showing Embodiment 5 of the present invention.

[0023] **Fig. 7** is a perspective diagram showing a conventional semiconductor pressure sensor.

[0024] **Fig. 8** is a circuit diagram showing a Wheatstone Bridge circuit formed on the diaphragm of **Fig. 7**.

DETAILED DESCRIPTION

[0025] ~~5. Best Mode for Carrying Out the Invention~~ Hereafter, the preferred embodiments of the present invention will be explained in detail.

[0026] The inventors of the present application performed various experiments to ~~develope~~ develop a semiconductor pressure sensor ~~which~~ that does not have a

fluctuation in an output. As a result, the inventors discovered that the fluctuation of a sensor output was brought on by an Fe (iron) atom among a number of metal-impuritiesy . That is, it is found that an Fe atom in a sensor chip is drawn to PN junctions such as a diffusion resistor resulting in producing a leak current or change in resistance value. If the metal-impurity represented by an Fe atom exists in active Si (silicon), it will be the condition that it is easy to narrow a band gap to excite an electron. And furthermore, when movable ions, such as Na (natrium), are interposed under bias application at high temperature, movement of an electron is promoted and it resultsing in the fluctuation.

[0027] Therefore, the fluctuation conditions of the sensor output are as follows:- (1) Existence existence of a metal-impurity, such as an Fe atom;- (2) Existence existence of movable ions, such as Na;- (3) Temperaturethe temperature is 125°C or more; and- (4) Application application of a bias potential. The fluctuation produces is produced when these four conditions are satisfied.

[0028] However, an Fe atom is hardly included in a usual CZ (Czochralski) wafer that is used. When a device is formed in a wafer, an Fe atom is considered to enter in the wafer. In the manufacture apparatus, iron and SUS (stainless alloy) are used in all parts. even Even a pincette is made from SUS. Therefore, in all processes, an Fe atom is considered to adhere to the wafer and to diffuse inside the wafer at various heat processes. Of course, although a precision cleaning in a furnace is performed before a heat process of the wafer in general, it is difficult to remove completely. This is similar also to an Na atom. There is a possibility that it may enter from all places, such as the human being's skin surface and perspiration. A complete removal is difficult.

[0029] Therefore, the inventors developed a semiconductor pressure sensor with the getter for capturing a metal-impurity, considering the above facts.

[Embodiment 1]

[0030] **Fig. 1** is a plan showing a semiconductor pressure sensor according to Embodiment 1 of the present invention. As shown in **Fig. 1**, a sensor chip 20 is made by n type silicon base 1. The whole center section except the circumference part of the silicon base 1 comprises a diaphragm 10 of a thin film. The diaphragmDiaphragm 10 is

provided with strain gauges 5a-5d made by p type diffusion resistors, ~~a~~ lead portion 6 formed by the p+ type diffusion resistors, ~~a~~ metal wiring 3, and terminals 4a-4d made from a metal. In this way, a Wheatstone Bridge circuit is formed from the above-mentioned components. When ~~the~~ silicon base 1 is an n type substrate, a diffusion resistor is formed by thermal diffusion or ion implantation of a boron or the like.

[0031] **Fig. 2A** is a sectional view along ~~the~~ A-A' line of **Fig. 1**. **Fig. 2B** is a sectional view along ~~the~~ B-B' line of **Fig. 1**. As shown in **Fig. 2A**, the main surface of ~~the~~ silicon base 1 is provided with ~~the~~ strain gauge 5a made from a p type diffusion layer, ~~the~~ lead portion 6 is made from a p+ type diffusion layer close to ~~the~~ strain gauge 5a, and ~~a~~ getter 8 made from a p+ type diffusion layer close to ~~the~~ lead portion 6.

[0032] And, ~~the~~ layer-insulation film 2 made from SiO_2 is provided on the main surface of ~~the~~ silicon base 1. ~~The metal~~Metal wiring 3, the terminal, etc. which comprise one part of such a Wheatstone Bridge circuit, are provided on the layer-insulation film 2. ~~The lead~~Lead portion 6 is electrically connected with ~~the~~ strain gauge 5a. Furthermore, ~~the~~ lead portion 6 is connected with ~~the~~ metal wiring 3 via ~~the~~ through-hole electrode 7 provided in ~~the~~ layer-insulation film 2. Moreover, as shown in **Fig. 2B**, ~~the~~ getter 8 is connected with ~~the~~ metal wiring 3 via ~~the~~ through-hole electrode 9 provided in ~~the~~ layer-insulation film 2. And, a reverse bias is applied to ~~the~~ getter 8 via terminal 4c.

[0033] Thus, in this embodiment, ~~the~~ getter 8, which has PN reverse bias potential, is provided in the vicinity of ~~the~~ strain gauges 5a-5d. Therefore, the metal-impurities in ~~the~~ silicon base 1 (Fe atom, Na atom, etc.) are captured ~~to~~ in a PN-junction area. In this way, the variation of the resistivity and the development of the leak current in ~~the~~ strain gauges 5a-5d are prevented.

[Embodiment 2]

[0034] **Fig. 3** is a top view showing a semiconductor pressure sensor according to Embodiment 2 of the present invention. ~~A getter~~Getter 8 is made into the mesh-like layout as shown in the diagram. Therefore, since a contact area of ~~the~~ p+ type getter 8 and ~~the~~ n type silicon substrate 1 ~~increases~~increase, namely, a PN-junction area is expanded, a gettering effect improves.

[Embodiment 3]

[0035] **Fig. 4** is a top view showing a semiconductor pressure sensor according to Embodiment 3 of the present invention. As shown in ~~the~~ **Fig. 4**, ~~A~~ getter 8 is locally provided only on the periphery of ~~the~~ strain gauges 5a-5d. Although ~~the~~ getter 8 in **Figs. 1** and **3** was provided over the main surface of ~~the~~ silicon substrate 1, a leak current increases with this formation so that ~~. So that,~~ there is a possibility that the power consumption of the entire chip may increase. Therefore, ~~the~~ getter 8 was locally provided on the periphery of ~~the~~ strain gauges 5a-5d such as in this embodiment. Of course, each getter is electrically connected with terminal 4c via ~~the~~ through-hole electrode 9. Therefore, PN reverse bias is applied to any getter.

[0036] In addition, in ~~the~~ **Fig. 4**, although each getter is connected by using an identical diffusion layer, instead of connecting by the diffusion layer, the metal wiring may be provided on ~~the~~ silicon substrate 1. Moreover, although the layout of ~~the~~ getter 8 is made into the shape of mesh, this invention includes the layout of the getter that is not made into the shape of mesh, such as in Embodiment 1.

[Embodiment 4]

[0037] **Fig. 5** is a top view showing a semiconductor pressure sensor according to Embodiment 4 of the present invention. As shown in ~~the~~ **Fig. 5**, a~~A~~ getter 8 is provided only on the periphery of ~~the~~ strain gauges 5c and 5d near a ground side. ~~Metal~~A metal-impurity, such as iron, ~~is~~ has positive ions. Therefore, it can be easy to draw to a portion with a large reverse bias to a substrate potential, i.e., sensor element of the ground side. If ~~the~~ getter 8 is more than required and is provided as ~~the above-~~ mentioned above, problems such as the increase of a leak current will be caused. Consequently, the increase of the power consumption of the entire chip can be prevented by providing the necessary minimum of getter ~~of necessary minimum~~ in the ground side (low potential side).

[0038] In addition, although the layout of ~~the~~ getter 8 is made in~~to~~ the shape of mesh, this invention includes the layout of the getter, which is not made in~~to~~ the shape of mesh such as in Embodiment 1.

[Embodiment 5]

[0039] **Fig. 6A, 6B,** and **6C** are the top views showing a semiconductor pressure sensor according to Embodiment 5 of the present invention. In ~~the~~ **Fig. 6A, 6B,** and **6C,** a getter has a plurality of the long and slender pattern ,which is ~~an~~ acutely angled toward a strain gauge. It is found that an Fe atom can be drawn to the edge of a diffusion resistor, i.e., PN-junction area. Consequently, it is effective if the layout of ~~a~~ getter 8 is performed so that PN-junction area can be ~~taken larger~~increased to the strain gauge as shown in ~~the Fig~~**Figs. 6A, 6B,** and **6C.**

[0040] As explained in the five embodiments, the present invention can capture the metal-impurity in a silicon substrate to prevent a leak current from being generat~~inged~~ by the work of the PN-junction area provided in the diaphragm.